Novoptel

Polarization scrambler/transformer module EPS1000

Revision history

Version	Date	Remarks	Author
0.9.7	13.08.2013	Draft version	R. Noé, B. Koch
0.9.8	01.08.2014	Extended SPI register description	B. Koch

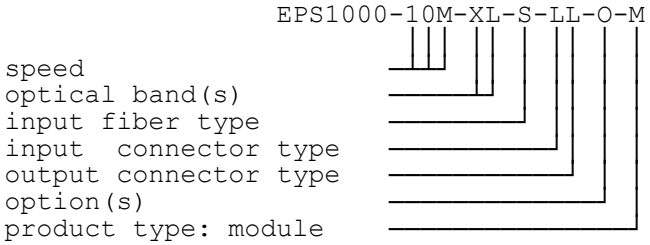
General description

The EPS1000 polarization scrambler/transformer modules comprises miniaturized, ultrafast, low-power optical polarization transformers (without feedback). They can be configured for a variety of purposes, namely polarization scrambling with rotating optical waveplates and the triggered or repetitive execution of a sequence of optical waveplate or driving voltage settings.

A daughterboard is available for optical power measurement (options O and OO). Simultaneous to the polarization transformer settings, optical intensities can thus be measured. This is useful for calibrated PDL measurements. Other components such as optical switches, digitally controlled variable optical attenuators and tap couplers can likewise be included.

The module runs from a single +5V supply. No logical connections are needed, nor any programming via JTAG port. For increased functionality, a few hard-wired logical lines are provided. Parameters may be set and read by two serial interfaces, SPI and UART. This accesses the full EPS1000 functionality. In a commercial test and measurement environment it is also recommended to connect the JTAG port, in order to allow firmware upgrades. In the desktop unit, the UART of the module is replaced by USB.

Ordering information



For example, the type EPS1000-10M-XL-S-LL-O-M can scramble polarization at up to 10 Mrad/s (20 Mrad/s with reduced accuracy), works from optical C to L band, has standard fiber at the optical input, has LC/UPC connectors and includes the option of optical power measurement.

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Novoptel reserves the right to change module and specifications.

Absolute maximum ratings

Parameter	Value	Remarks/Conditions
Supply voltage	−0.3...+5.5 V	
Voltage at all logical ports	−0.3...+3.6 V	
Optical input power at any port	+20 dBm	
Storage temperature	−40...+85°C	
Operating temperature	−10...+70°C	

Characteristics

Parameter	Value	Remarks/Conditions
Wavelength range (covered if letter is included in part number)	1529...1562 nm	C = optical C band
	1529...1568 nm	X = extended optical C band
	1568...1610 nm	L = optical L band. 1625 nm upper limit is under consideration.
	tbd ...1529 nm	S = optical S band
	1310 nm	3 = optical 1310 nm band (range tbd)
Optical input power for optical power measurement	−11 dBm or tbd	Only valid with options O and OO. The scrambler input power is independent of this.
Optical insertion loss	1.5...3 dB (typically 2.5 dB)	From optical scrambler input to optical output.
Maximum polarization scrambling speed of halfwave plate (HWP)	10 Mrad/s or tbd	Scrambling at up to 20 Mrad/s is possible with reduced accuracy. Speed may be reduced at corners of operating temperature range.
Maximum polarization scrambling speed of quarterwave plates (QWPs)	1 Mrad/s or tbd	
Supply voltage	+4.75...5.25 V	
Supply current	1.4...1.7 A or tbd 2.1...2.5 A or tbd	For 10 Mrad/s version at low scrambling speeds. For 10 Mrad/s version operated at 20 Mrad/s. Versions with reduced maximum polarization scrambling speed and supply current are also available.
Logical port levels	LVCMOS33	3.3 V CMOS logic

Type of optical input

Type	Function
S	Standard singlemode fiber. Standard version.
P	Polarization-maintaining fiber (PANDA). This may be useful in scenarios where an optical source with polarization-maintaining fiber is connected to the EPS1000.

Connector types

Type	Function
N	none
F	FC/UPC
A	FC/APC
L	LC/UPC
S	SC/PC
E	E2000

First letter specifies input connector, second letter specifies output connector(s).

Options

Type	Function
O	Optical power measurement. Simultaneous to the polarization transformer settings, optical intensities can thus be measured. A back-to-back measurement permits one to determine

	the polarization-dependent loss of the EPS1000. Subsequently, calibrated PDL (or simply loss) measurements of a device under test are possible. The optical power range can be increased by different input attenuations, to be set by a variable attenuator or the insertion of a fixed attenuator. An optical switch can also be included in the desktop version.
OO	Like option O, but 2 optical inputs are provided, selectable by a fast electronic switch. This allows for ratiometric measurements without optical reconfiguration. A tap coupler can also be included and spliced.
N	None. Space is available for a small daughterboard, the connections of which are detailed upon request.
	More digital inputs/outputs and analog inputs are available on the EPS1000 module. This means that other components such as digitally controlled variable optical attenuators and optical switches can be connected and operated by the user. One example is a variable optical attenuator at the input of an EPS1000 with option O, which increases the dynamic range of loss measurement. Details upon request.

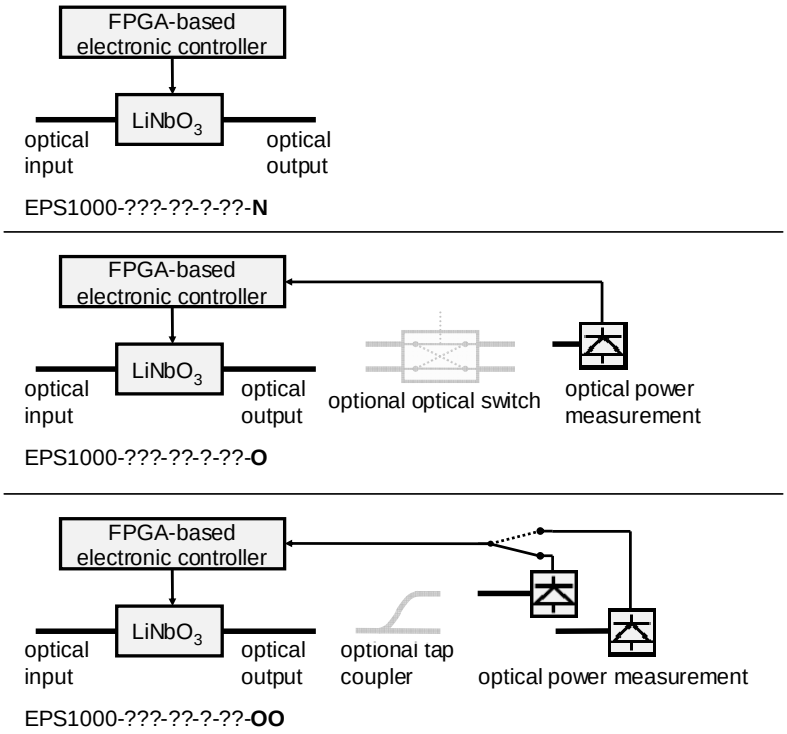


Fig. 1: Simplified block diagram for various configurations, and associated ordering codes

Electrical connector

Nr.	Name	I/O	Logic	Description
1	RE1	I/O	LVCMOS33	Reserved (2)
2	URXD	I/O	LVCMOS33	UART RXD. For parameter setting.
3	ABS	O	LVCMOS33	Module Absent. High level "1" is module absent, low level (0) is module present. Pull-up resistor (e.g., 10 kOhm to +3.3 V) on host card is therefore needed (3). On the module ABS will be connected to an FPGA output that is permanently set to low level "0". (Note: Therefore, during reset, the FPGA output will have high impedance and the pull-up resistor on the host card will pull ABS high "1" for a short time. It would be more logical to provide a galvanic connection of ABS to ground in the module. But the chosen solution is more versatile, because ABS could be re-programmed to get another function (like RE1...RE8).)
4	**+5V**	--	--	**+5 V supply voltage**
5	SDO	O	LVCMOS33	SPI Data Out. For parameter setting.
6	**+5V**	--	--	**+5 V supply voltage**
7	+3.3V	--	--	+3.3 V. Can be used to power an external JTAG cable. Do not apply externally generated voltage here. (1)

8	RE2	I/O	LVCMOS33	Reserved (2)
9	RE3	I/O	LVCMOS33	Reserved (2)
10	TCK	I	LVCMOS33	JTAG. For firmware upgrade.
11	RE4	I/O	LVCMOS33	Reserved (2)
12	TMS	I	LVCMOS33	JTAG. For firmware upgrade.
13	CS	I	LVCMOS33	SPI Enable. For parameter setting.
14	TDI	I	LVCMOS33	JTAG. For firmware upgrade.
15	RE5	I/O	LVCMOS33	Reserved (2)
16	SDCK	I	LVCMOS33	SPI Data Clock. For parameter setting.
17	**GND**	**--**	**--**	**Ground**
18	SDI	I	LVCMOS33	SPI Data In. For parameter setting.
19	**GND**	**--**	**--**	**Ground**
20	TDO	O	LVCMOS33	JTAG. For firmware upgrade.
21	**GND**	**--**	**--**	**Ground**
22	TRGIO	I/O	LVCMOS33	Trigger input/output in synchronous/triggered scrambling mode
23	RE6	I/O	LVCMOS33	Reserved (2)
24	RE7	I/O	LVCMOS33	Reserved (2)
25	UTXD	I/O	LVCMOS33	UART TXD. For parameter setting.
26	RE8	I/O	LVCMOS33	Reserved (2)
27	RE9	I/O	LVCMOS33	Reserved (2)
28	RE10	I/O	LVCMOS33	Reserved (2)
29	RE11	I/O	LVCMOS33	Reserved (2)
30	RE12	I/O	LVCMOS33	Reserved (2)
31	RE13	I/O	LVCMOS33	Reserved (2)
32	RE14	I/O	LVCMOS33	Reserved (2)
33	RE15	I/O	LVCMOS33	Reserved (2)
34	RE16	I/O	LVCMOS33	Reserved (2)
35	RE17	I/O	LVCMOS33	Reserved (2)
36	RE18	I/O	LVCMOS33	Reserved (2)
37	RE19	I/O	LVCMOS33	Reserved (2)
38	RE20	I/O	LVCMOS33	Reserved (2)
39	RE21	I/O	LVCMOS33	Reserved (2)
40	RE22	I/O	LVCMOS33	Reserved (2)

(1) Generated by internal voltage regulators.

(2) For possible future use. Connections to I/O pins of a programmable controller are therefore recommended for RE1 to RE8. These I/O pins of the programmable controller should be set to the high-impedance state. (More of RE9 to RE22 may, but need not, be connected to the controller.)

(3) Except for this pin, no external pull-up or pull-down resistors are needed. As far as required, pull-up and pull-down resistors are already implemented on the module.

Power connector

Nr.	I/O
1	GND
2	+5V
3	+5V
4	–Fan

Not needed in an environment where the electrical connector is plugged into a motherboard and cooling airflow is provided.
Recommended if a ribbon cable is used to connect the main electrical connector, in order to reduce ohmic losses. Power is applied at pins 1 and 2. Between pins 4 (negative) and 3 (positive) a 5-V cooling fan with a current of up to 2 A can be connected. It is switched on automatically when the module card needs cooling. With appropriate air ducting, even a 1-W fan is sufficient. A freewheeling diode toward pin 3 (+5V) protects pin 4 (–Fan) against overvoltages during off-switching. A fan is not needed if the user takes otherwise care that the module card stays below +75°C. Normally this is easy, given the low power consumption of the module card.
On the module card there is a reverse polarity protection diode Vishay 12CWQ03F http://www.vishay.com/docs/94132/12cwq03f.pdf (two diode sections connected in parallel). But since

many components on the module card are specified to support only voltages down to −0.3 V one must not at all rely on this! Limiting the maximum supply current can help the module card to survive inadvertedly applied reverse voltage.

Serial peripheral interface (SPI)

The module starts operation without SPI. The user doesn't have to use the SPI at all. While the module starts operation without SPI, this serial interface can be used to control function, modify parameters, read back these commands as well as debug register contents.

Transmission starts with falling edge of CS and ends with rising edge of CS. After falling edge of CS, the command is transmitted. SDI is sampled with rising edge of SCK. Maximum SCK frequency is 500 kHz. Command and data word length is 16 bit each. MSB of command and data word is sent first, LSB last. If a valid *register read* (RDREG) command is received, the SDO output register shifts with falling edge of SCK to transmit the requested data word. Otherwise SDO remains in high impedance state. Data transfer to the device continues directly after transmitting a *register write* (WRREG) command.

Each SPI register has 16 bit. Upon power-on, all registers are reset to default.

For a possible remote debugging, content of all defined registers needs to be read and sent to Novoptel.

All registers in the 12-bit address space that are not defined below are reserved, and should not be written into!

Serial peripheral interface (SPI) commands

Command	Code	Data	Function
RDREG	0XXXh	OUT	Read register XXXh (for definition see below)
WRREG	1XXXh	IN	Write register XXXh (for definition see below)

Serial peripheral interface (SPI) registers

Register address	Bit(s)	Read/ Write	Function
0	0	R/W	HWP rotation enable(1) or disable (0)
0	1	R/W	HWP direction backward(1) or forward(0)
1	0	R/W	QWP0 rotation enable(1) or disable (0)
1	1	R/W	QWP0 direction backward(1) or forward(0)
2	0	R/W	QWP1 rotation enable(1) or disable (0)
2	1	R/W	QWP1 direction backward(1) or forward(0)
3	0	R/W	QWP2 rotation enable(1) or disable (0)
3	1	R/W	QWP2 direction backward(1) or forward(0)
4	0	R/W	QWP3 rotation enable(1) or disable (0)
4	1	R/W	QWP3 direction backward(1) or forward(0)
5	0	R/W	QWP4 rotation enable(1) or disable (0)
5	1	R/W	QWP4 direction backward(1) or forward(0)
6	0	R/W	QWP5 rotation enable(1) or disable (0)
6	1	R/W	QWP5 direction backward(1) or forward(0)
9	15..0	R/W	HWP rotation speed Bits 15..0[(1)]
10	15..0	R/W	HWP rotation speed Bits 31..16[(1)]
11	15..0	R/W	QWP0 rotation speed Bits 15..0[(2)]
12	15..0	R/W	QWP0 rotation speed Bits 31..16[(2)]
13	15..0	R/W	QWP1 rotation speed Bits 15..0[(2)]
14	15..0	R/W	QWP1 rotation speed Bits 31..16[(2)]
15	15..0	R/W	QWP2 rotation speed Bits 15..0[(2)]
16	15..0	R/W	QWP2 rotation speed Bits 31..16[(2)]
17	15..0	R/W	QWP3 rotation speed Bits 15..0[(2)]
18	15..0	R/W	QWP3 rotation speed Bits 31..16[(2)]
19	15..0	R/W	QWP4 rotation speed Bits 15..0[(2)]
20	15..0	R/W	QWP4 rotation speed Bits 31..16[(2)]

21	15..0	R/W	QWP5 rotation speed Bits 15..0[2]
22	15..0	R/W	QWP5 rotation speed Bits 31..16[2]
25	15..0	R/W	Optical frequency Index I[3]
26	15..0	R/W	Current optical frequency band index
27	15..0	R/W	Current optical center wavelength
40	15..0	R/W	HWP position Index I[4]
41	15..0	R/W	QWP0 position index I[4]
42	15..0	R/W	QWP1 position index I[4]
43	15..0	R/W	QWP2 position index I[4]
44	15..0	R/W	QWP3 position index I[4]
45	15..0	R/W	QWP4 position index I[4]
46	15..0	R/W	QWP5 position index I[4]
47	15..0	R	Internal table current position dwell time in multiples of 40 ns; Bits 15..0
48	15..0	R	Internal table current position dwell time in multiples of 40 ns; Bits 31..16
50	13..0	R/W	$LiNbO_3$ section 1 electrode 1 voltage[5]
51	13..0	R/W	$LiNbO_3$ section 1 electrode 2 voltage[5]
52	13..0	R/W	$LiNbO_3$ section 2 electrode 1 voltage[5]
53	13..0	R/W	$LiNbO_3$ section 2 electrode 2 voltage[5]
54	13..0	R/W	$LiNbO_3$ section 3 electrode 1 voltage[5]
55	13..0	R/W	$LiNbO_3$ section 3 electrode 2 voltage[5]
56	13..0	R/W	$LiNbO_3$ section 4 electrode 1 voltage[5]
57	13..0	R/W	$LiNbO_3$ section 4 electrode 2 voltage[5]
58	13..0	R/W	$LiNbO_3$ section 5 electrode 1 voltage[5]
59	13..0	R/W	$LiNbO_3$ section 5 electrode 2 voltage[5]
60	13..0	R/W	$LiNbO_3$ section 6 electrode 1 voltage[5]
61	13..0	R/W	$LiNbO_3$ section 6 electrode 2 voltage[5]
62	13..0	R/W	$LiNbO_3$ section 7 electrode 1 voltage[5]
63	13..0	R/W	$LiNbO_3$ section 7 electrode 2 voltage[5]
64	13..0	R/W	$LiNbO_3$ section 8 electrode 1 voltage[5]
65	13..0	R/W	$LiNbO_3$ section 8 electrode 2 voltage[5]
80	13..0	R	Summary of all wave plates rotation enable and direction status
84	15..0	R	Firmware version as 4 digit BCD
85	15..0	R	Device DNA word 3 (DNA bits 63...48) (same as read via JTAG)
86	15..0	R	Device DNA word 3 (DNA bits 47...32) (same as read via JTAG)
87	15..0	R	Device DNA word 3 (DNA bits 31...16) (same as read via JTAG)
88	15..0	R	Device DNA word 3 (DNA bits 15...0) (same as read via JTAG)
89	15..0	R	$LiNbO_3$ Device Number (bits 31…16)
90	15..0	R	$LiNbO_3$ Device Number (bits 15…0)
91	15..0	R	EPS Unit Serial Number
96-111	15..0	R	Module type code as 32 character string. Beginning at 060h, each Register contains two bytes, representing two ASCII-coded characters.
123	15..0	R	Darc current offset of optional photodetector
124	15..0	R	Optical power of optional photodetector at upper range limit in µW
128	15..0	R	Integral part of ADC sample
129	9..0	R/W	Averaging Time Exponent (ATE) for ADC sample
130	15..0	R/W	Address of internal sampling memory
131	15..0	R	Data-Out of internal sampling memory
132	0	R/W	Timed output enable (1) or disable (0)
133	15..0	R	Fractional part of ADC sample, frozen at each reading of register 128
134	15..0	R/W	Maximum memory address for measurements
135	15..0	R	Current memory address during measurements
181	12..0	R	Current module temperature in °C*2^4
190	15..0	R	Number of supported frequency bands
191	15..0	R	Center wavelength of frequency band 1
192	15..0	R	Maximum frequency in frequency band 1 in THz * 2^7
193	15..0	R	Minimum frequency in frequency band 1 in THz * 2^7
194	15..0	R	Maximum frequency index in frequency band 1

195	15..0	R	Start frequency index in frequency band 1
196	15..0	R	Center wavelength of frequency band 2
197	15..0	R	Maximum frequency in frequency band 2 in THz * 2^7
198	15..0	R	Minimum frequency in frequency band 2 in THz * 2^7
199	15..0	R	Maximum frequency index in frequency band 2
200	15..0	R	Start frequency index in frequency band 2
201-215	15..0	R	Reserved for 3 more frequency bands
216	15..0	R	Current table row
217	0	R	Indicates a trigger event in the past second
218	0	R/W	Sync mode: Table mode (0) or row mode (1)
219	9..0	R/W	Table memory address (0…1023)
220	0	R/W	Continuous table execution: Disabled (0) or enabled (1)
221	0	W	Table memory write enable. Disabled (0) or enabled (1)
222	15..0	R/W	Table row execution time in multiples of 40 ns; Bits 15..0
223	15..0	R/W	Table row execution time in multiples of 40 ns; Bits 31..16
224	0	R/W	External trigger source enable. Disabled (0) or enabled (1)
225	0	R/W	Internal trigger source: Periodic counter. Disabled (0) or enabled (1)
225	1	R/W	Internal trigger source: ATE synchronous. Disabled (0) or enabled (1)
226	0	R/W	Trigger output enable: Disabled (0) or enabled (1)
227	0	W	Manual trigger event
228	9..0	R/W	Table length (0…1023)
229	0	R/W	Sync mode enable. Disabled (0) or enabled (1)
230	15..0	R/W	QWP0 position input for internal table memory
231	15..0	R/W	QWP1 position input for internal table memory
232	15..0	R/W	QWP2 position input for internal table memory
233	15..0	R/W	HWP position input for internal table memory
234	15..0	R/W	QWP3 position input for internal table memory
235	15..0	R/W	QWP4 position input for internal table memory
236	15..0	R/W	QWP5 position input for internal table memory
237	15..0	R/W	Table row execution time bits 15...0 input for internal table memory
238	15..0	R/W	Table row execution time bits 31...16 input for internal table memory
240	15..0	R	QWP0 position output of internal table memory
241	15..0	R	QWP1 position output of internal table memory
242	15..0	R	QWP2 position output of internal table memory
243	15..0	R	HWP position output of internal table memory
244	15..0	R	QWP3 position output of internal table memory
245	15..0	R	QWP4 position output of internal table memory
246	15..0	R	QWP5 position output of internal table memory
247	15..0	R	Table row execution time bits 15...0 output of internal table memory
248	15..0	R	Table row execution time bits 31...16 output of internal table memory
250	15..0	R/W	$LiNbO_3$ section 1 electrode 1 voltage for internal table memory
251	15..0	R/W	$LiNbO_3$ section 1 electrode 2 voltage for internal table memory
252	15..0	R/W	$LiNbO_3$ section 2 electrode 1 voltage for internal table memory
253	15..0	R/W	$LiNbO_3$ section 2 electrode 2 voltage for internal table memory
254	15..0	R/W	$LiNbO_3$ section 3 electrode 1 voltage for internal table memory
255	15..0	R/W	$LiNbO_3$ section 3 electrode 2 voltage for internal table memory
256	15..0	R/W	$LiNbO_3$ section 4 electrode 1 voltage for internal table memory
257	15..0	R/W	$LiNbO_3$ section 4 electrode 2 voltage for internal table memory
258	15..0	R/W	$LiNbO_3$ section 5 electrode 1 voltage for internal table memory
259	15..0	R/W	$LiNbO_3$ section 5 electrode 2 voltage for internal table memory
260	15..0	R/W	$LiNbO_3$ section 6 electrode 1 voltage for internal table memory
261	15..0	R/W	$LiNbO_3$ section 6 electrode 2 voltage for internal table memory
262	15..0	R/W	$LiNbO_3$ section 7 electrode 1 voltage for internal table memory
263	15..0	R/W	$LiNbO_3$ section 7 electrode 2 voltage for internal table memory
264	15..0	R/W	$LiNbO_3$ section 8 electrode 1 voltage for internal table memory
265	15..0	R/W	$LiNbO_3$ section 8 electrode 2 voltage for internal table memory
270	15..0	R	$LiNbO_3$ section 1 electrode 1 voltage, output of internal table memory

271	15..0	R	$LiNbO_3$ section 1 electrode 2 voltage, output of internal table memory
272	15..0	R	$LiNbO_3$ section 2 electrode 1 voltage, output of internal table memory
273	15..0	R	$LiNbO_3$ section 2 electrode 2 voltage, output of internal table memory
274	15..0	R	$LiNbO_3$ section 3 electrode 1 voltage, output of internal table memory
275	15..0	R	$LiNbO_3$ section 3 electrode 2 voltage, output of internal table memory
276	15..0	R	$LiNbO_3$ section 4 electrode 1 voltage, output of internal table memory
277	15..0	R	$LiNbO_3$ section 4 electrode 2 voltage, output of internal table memory
278	15..0	R	$LiNbO_3$ section 5 electrode 1 voltage, output of internal table memory
279	15..0	R	$LiNbO_3$ section 5 electrode 2 voltage, output of internal table memory
280	15..0	R	$LiNbO_3$ section 6 electrode 1 voltage, output of internal table memory
281	15..0	R	$LiNbO_3$ section 6 electrode 2 voltage, output of internal table memory
282	15..0	R	$LiNbO_3$ section 7 electrode 1 voltage, output of internal table memory
283	15..0	R	$LiNbO_3$ section 7 electrode 2 voltage, output of internal table memory
284	15..0	R	$LiNbO_3$ section 8 electrode 1 voltage, output of internal table memory
285	15..0	R	$LiNbO_3$ section 8 electrode 2 voltage, output of internal table memory

(1) The HWP rotation speed index I (32 bit integer) is calculated from the nominal HWP rotation speed SHWP (in krad/s) by I = round(SHWP·100).
(2) The QWP rotation speed index I (32 bit integer) is calculated from the nominal QWP rotation speed SQWP (in rad/s) by I = round(SQWP·100).
(3) The optical frequency index I is calculated from the optical frequency F (in THz) by I=round(F·10-1829).
(4) The position index I is calculated from Position P (in degrees) by I=round(P·65536/360).
(5) Only applicable since firmware 1.0.2.0. An offset of 8192 corresponds to 0 Volt, the upper and lower limitations of 8192±6000 correspond to ±45 Volt.

Serial peripheral interface (SPI) timing

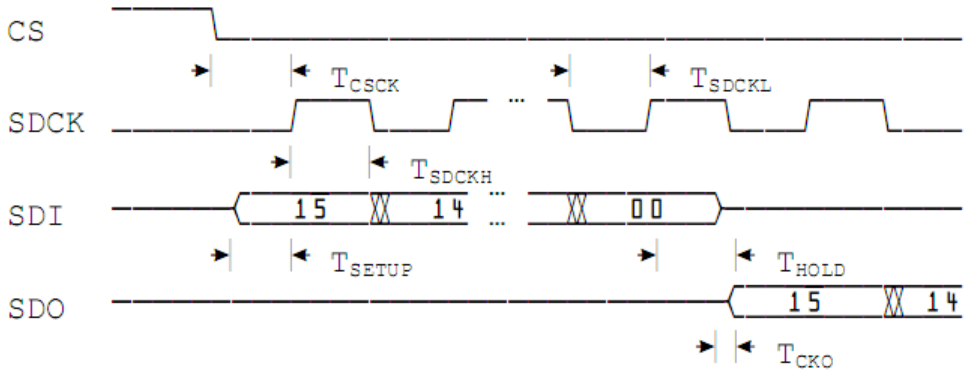


Fig. 2: Timing of SPI port.

Symbol	Description	Min	Max	Units
T_{CSCK}	CS low to SDCK high	120	–	ns
T_{CKCS}	SDCK low to CS high	120	–	ns
T_{SDCKL}	SDCKL low time	1	–	µs
T_{SDCKH}	SDCKL high time	1	–	µs
T_{SETUP}	SDI egde to SDCK high (setup time)	30	–	ns
T_{HOLD}	SDCK to SDI edge (hold time)	30	–	ns
T_{CKO}	SDCK edge to stable SDO	–	100	ns

UART interface

All SPI registers described above can also be accessed via an UART interface. Only electrical connectors 2 (RXD) and 25 (TXD) are required, without RTS and CTS hardware handshaking. The UART configuration is as follows:

Baud Rate	230400 baud
Word Length	8 Bits

Stop Bits	1 Bit
Parity	0 Bit

UART transfer protocol

All communication is initiated by the host, e.g. the connected Microcontroller. Writing to a register uses a 9 byte data packet. Each byte represents an ASCII-coded character. The packet starts with the ASCII-character “W” and ends with the ASCII-code for carriage return:

“W”	A(2)	A(1)	A(0)	D(3)	D(2)	D(1)	D(0)	^CR

The 12 bit register address A is sent using 3 bytes, each containing the ASCII-character of the hexadecimal numbers 0 to F which represents the 4 bit nibble. The character of the most significant nibble is sent first. The 16 bit data, which should be written into the register, is sent with 4 bytes using the same coding as the register address.

Reading data from a register requires the host to send a request data packet to the instrument. The packet starts with the ASCII-character “R”, followed by the register address coded the same way as in write data packets:

“R”	A(2)	A(1)	“0”	“0”	“0”	“0”	“0”	^CR

After receiving the request data packet, the instrument sends the requested data packet to the host:

D(3)	D(2)	D(1)	D(0)	^CR

Firmware upgrading

Via the JTAG port the user can upgrade the firmware. Note that the upgrading firmware must be obtained from Novoptel on a per-module basis because the firmware is encrypted and authenticated. For this purpose, Novoptel needs to be told the device DNA of the FPGA, which also serves as the serial number of the module. The user can find out the device DNA remotely via SPI (as long as the firmware is working) or via JTAG (in any case, which is therefore recommended). During firmware upgrading, polarization control is not possible.

The schematic and timing of the JTAG port correspond to that detailed in Spartan-3 Generation Configuration User Guide UG332 (v1.6) October 26, 2009 from Xilinx (www.xilinx.com). A schematic is given in Fig. 3.

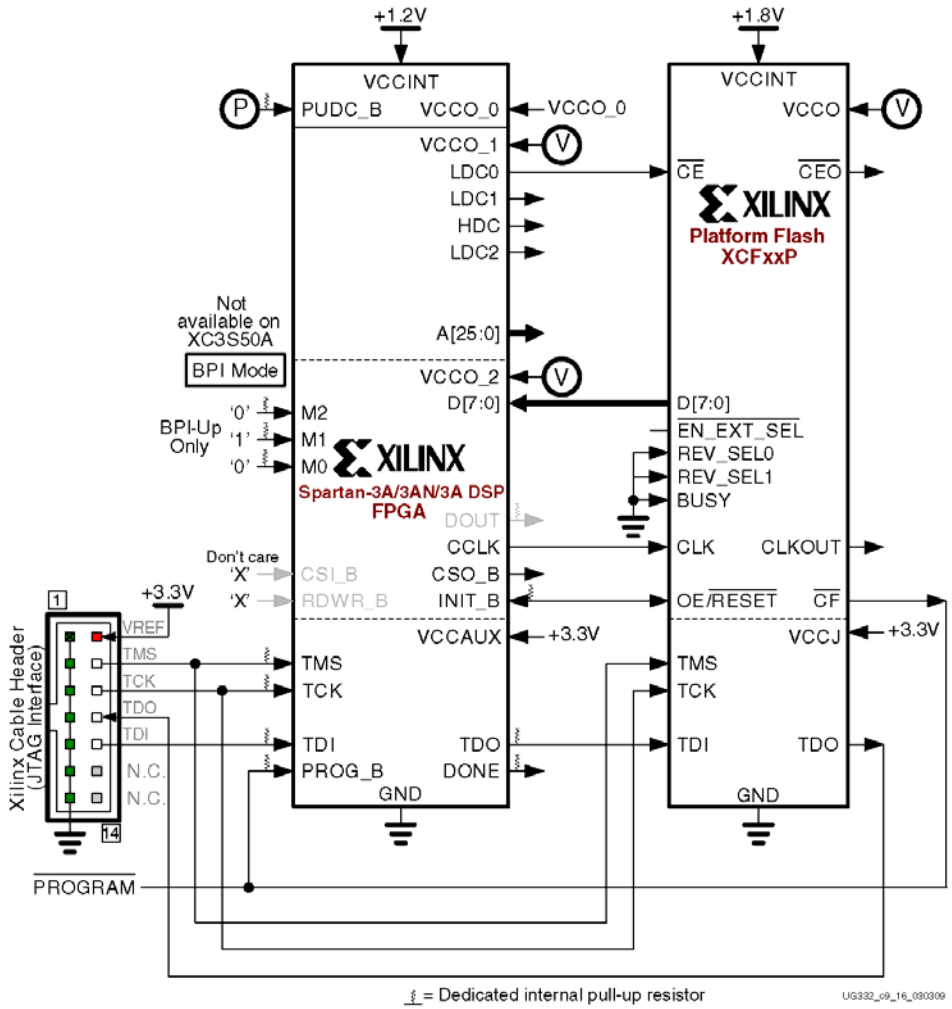


Figure 5-6: **Master BPI Mode Using Xilinx Parallel Platform Flash PROMs (XCFxxP)**

- The diagram in Figure 5-6 shows an Extended Spartan-3A family FPGA, but the same approach also works with Spartan-3E FPGAs.
- The Xilinx Parallel Platform Flash PROM family is in-system programmable using JTAG, similar to the FPGA.
- See XAPP483, *Multiple-Boot with Platform Flash PROMs*
- The FPGA's LDC2, LDC1, LDC0, and HDC outputs actively drive during configuration. Use the LDC0 output to enable the Platform Flash PROM during

Fig. 3: Schematic of JTAG port, adopted from Xilinx. However, instead of the Xilinx Cable Header the JTAG connections are part of the module connector.

JTAG Timing

Fig. 4 shows timing definitions of the JTAG port signals (source: Platform Flash Product Specification DS123 (v2.16) November 14, 2008 from XILINX (www.xilinx.com)).

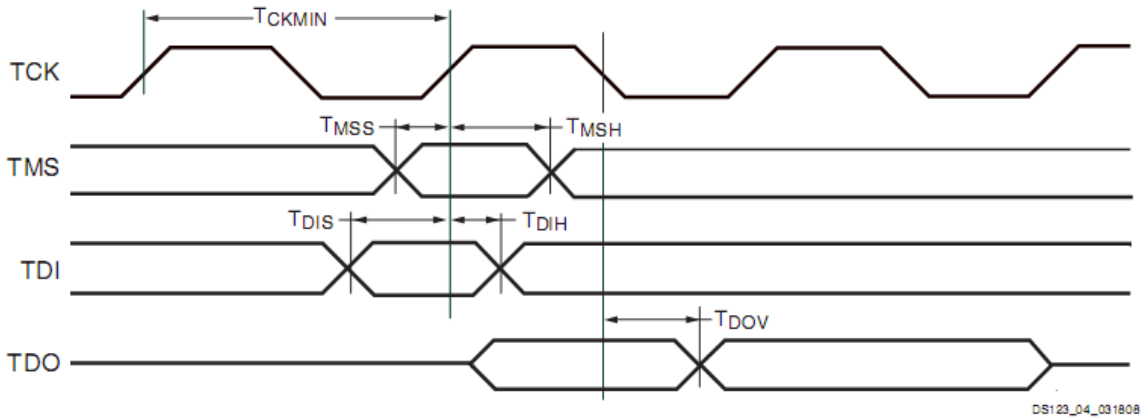


Fig. 4: Timing of JTAG port, adopted from Xilinx.

Symbol	Description	Min	Max	Units
T_{CKMIN}	TCK minimum clock period	67	–	ns
T_{MSS}	TMS setup time	8	–	ns
T_{MSH}	TMS hold time	25	–	ns
T_{DIS}	TDI setup time	8	–	ns
T_{DIH}	TDI hold time	25	–	ns
T_{DOV}	TDO valid delay	–	22	ns

Mechanical outline and mounting

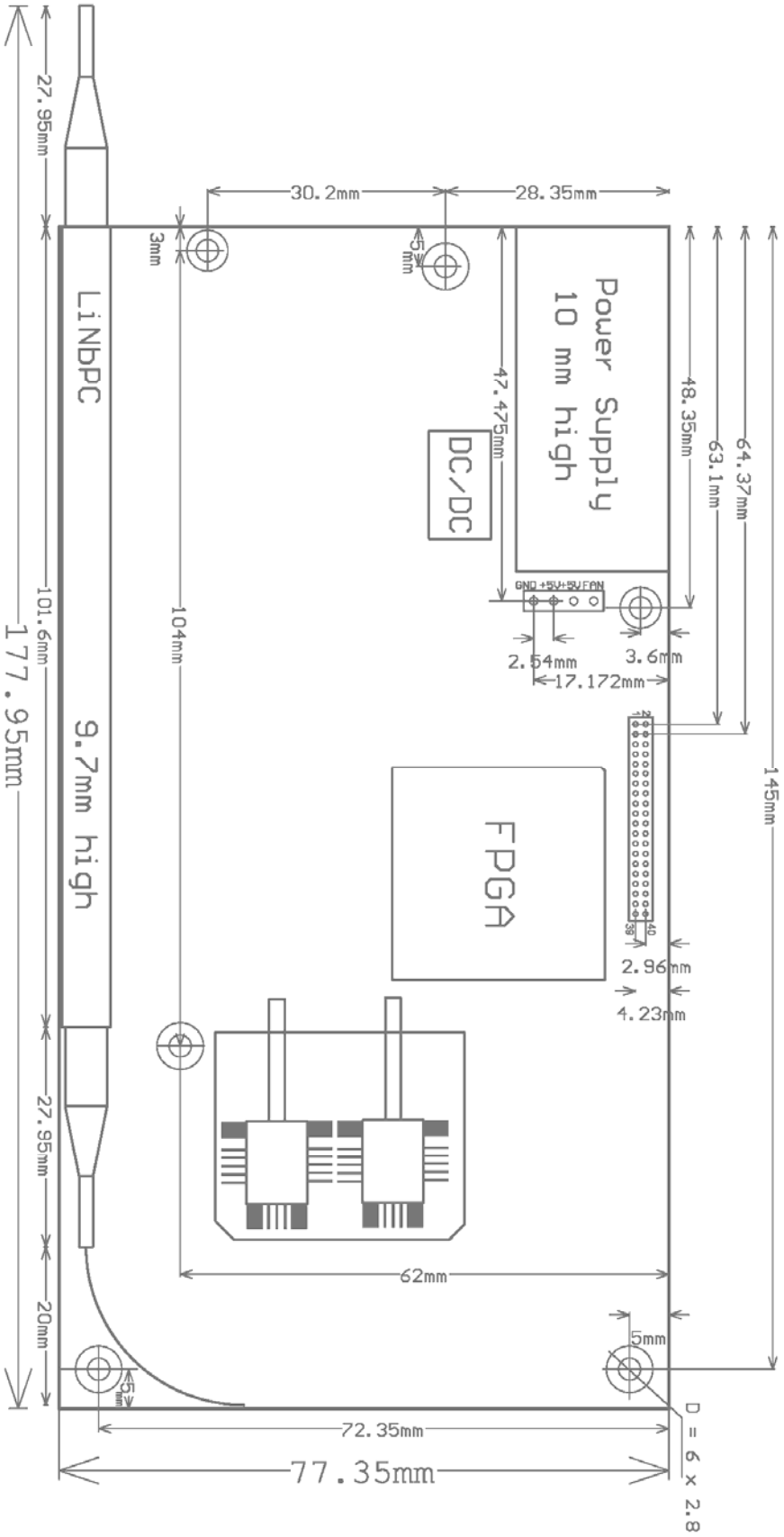


Fig. 5: Mechanical drawing of module card, seen from top

Airflow should preferably be parallel to the long and high $LiNbO_3$ polarization transformer (i.e., vertical in Fig. 5).

The default connector on the module card is Harwin M50-3152042 (http://www.harwin.com/search/M50-315?ProductSearch=True).

Referring to Fig. 5, the default connector mounting position is at the bottom of the board. A suitable mating piece on the host card is M50-3501242 (http://www.harwin.com/search/M50-350?ProductSearch=True). It connects to pins 1...24. If the UART is to be used for parameter setting M50-3501342 is needed. It connects to pins 1...26. Longer connectors up to M50-3502042 can also be used but this is not necessary. The combination M50-3152042 M50-3501242 achieves a total separation of module card and host card of 3.2 mm. Alternatively, if on the host card M50-3501242 is replaced by M50-3601242 then the separation of module card and host card becomes 3.9 mm.

Upon request, an additional Harwin M50-3152042 connector can be mounted at the top of the module card. A ribbon cable connector like Samtec FFMD-20-... (http://www.farnell.com/datasheets/452598.pdf) may be plugged in there. Total height above the module card is on the order of 7.3 mm. Ribbon cable connectors have large ohmic losses. Therefore on top of such module cards there is an extra angled +5 V and GND, 5-pin power connector with 2.54 mm pitch.

In any case, pin numbers of module connector are defined per Figs. 5, 6, which depict the module card from above.

Care and appropriate mechanical support must be applied when connecting or disconnecting the connectors, in order not to bend the module card so much that components or solder dots can break.

Other connectors can be supplied upon request. For example, if on module card M50-3152042 is replaced by M50-3122045 this brings the separation between module card and host card to 4.6 mm (with M50-3501242 on host card) or 5.3 mm (with M60-3501242 on host card).

If a separation of module card and host card of 3.2 mm is chosen the total module height above the host card will be $\leq$ 16 mm. Component height at the bottom of the module card (within the 3.2 mm separation) is on the order of 2 mm.

The six 2.8 mm mounting holes, and surrounding areas with about 5.2 mm (on one hole) or 5.9 mm (on the other five holes) diameter on both sides of the module card, are metallized and connected to ground potential. This allows mounting the card with metal spacers on the host card, for example 3.2 (or 3.9) mm long aluminum cylinders with 4.7 mm diameter and centric 2.6 mm holes. All mounting holes can accomodate M2.5 hexagon spacer bolts (~4.6 mm maximum width). See legend of Fig. 7.

Galvanic connections to the ground plane of the host card not only through the connector but also through the mounting holes are recommended, in order to shield the signals at the bottom of the module card. In order to avoid short circuits under mechanical bending, the ground plane on the host card should be isolated (by a solder stop mask), except for the mounting hole and connector places.

If the host card presents toward the host card not only a ground plane but also components then a grounded shielding plane is recommended between module card and host card. Indeed an optional metal case is under consideration. This will may be a metal cover and a metal bottom plate, with air holes and openings for fibers and electrical connector. Cover and bottom plate are screwed onto the board together with metal spacers, thereby getting connected to ground and forming a fairly well shielded enclosure.

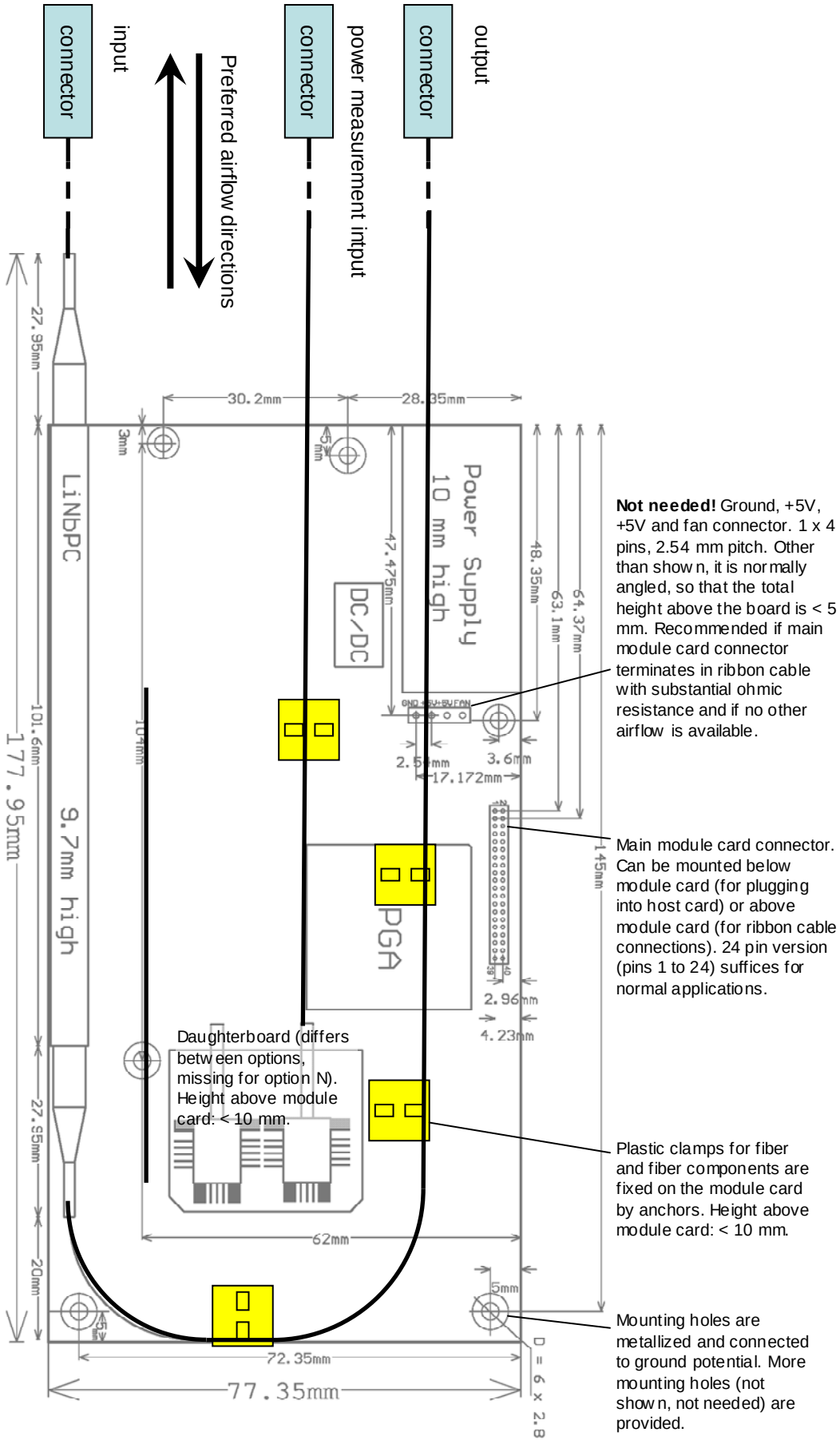


Fig. 6: Approximate fiber layout (shown with option O for optical power measurement)

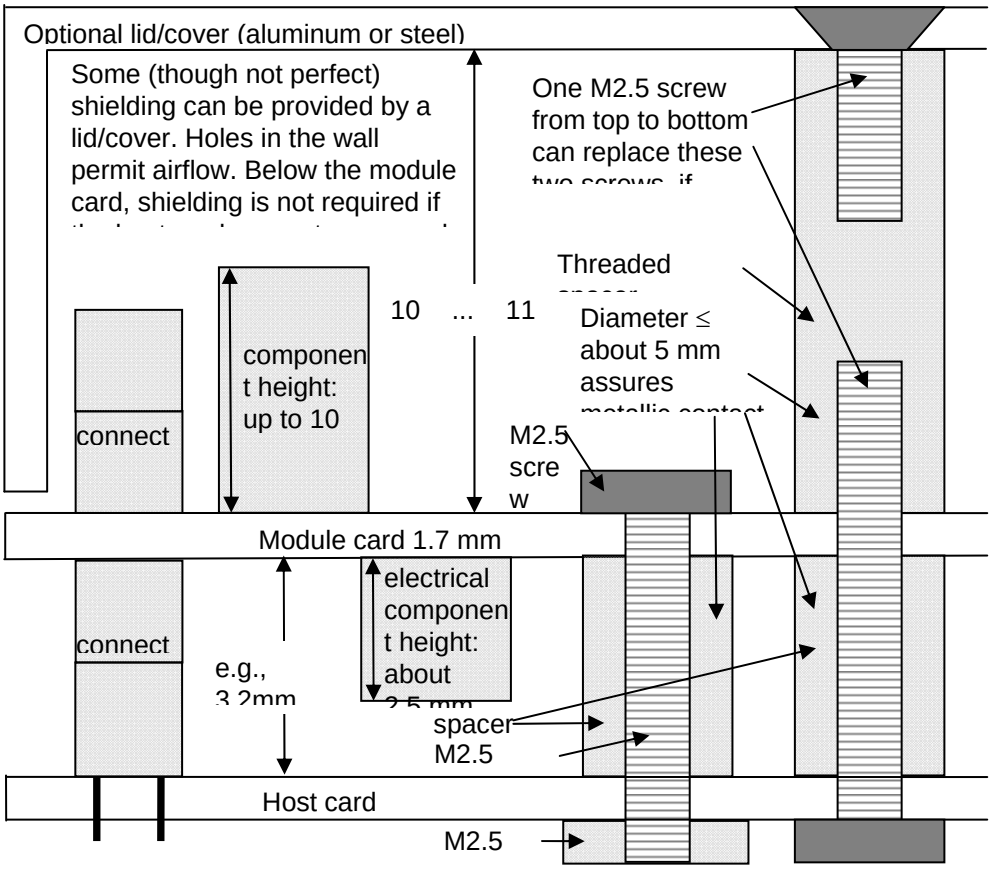


Fig. 7: Schematic (not to scale) of cross section, showing the connection to a host card and a choice of mounting possibilities. – The 5.9 mm diameter metallizations of five mounting holes suffice to accomodate M2.5 nuts (~5.6 mm maximum width). The mounting hole which is nearest to the optical input fiber (top left in Figs. 5, 6) has only 5.2 mm diameter metallizations and does not accomodate M2.5 nuts, only M2.5 screw heads (~4.5 mm diameter, as sketched for left mounting screw), or simply an M2.5 hexagon spacer bolt, or possibly an M2.5 nut on top of a spacer disc with 5.0 mm outer diameter.

Miscellaneous

This module is designed for industrial applications only. It must not be used if human life depends on its correct functioning (e.g., medical applications).

Installation and use of the module have to comply with the corresponding regulations for the operation of electrical and optical installations of the country where the module is to be used.

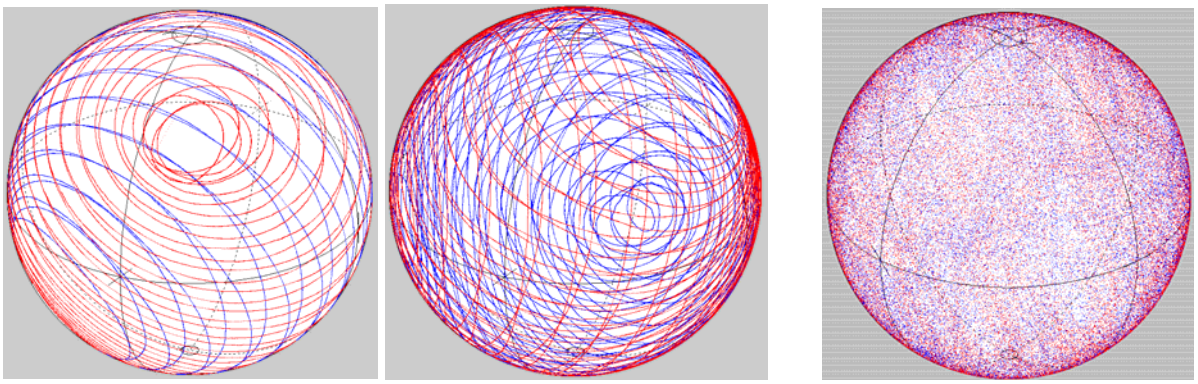
Diversion contrary to German law is prohibited. In addition, diversion contrary to USA law is prohibited. Module hardware is subject to compliance with all United States Export Administration Regularities. USA Regulations prohibit the transfer or reexport of module hardware, directly or indirectly, to restricted countries or entities.

You or anybody to whom you grant access may not reverse engineer, disassemble, decompile or decode the module, its hardware and software, except and only to the extent that such activity is expressly permitted by applicable law notwithstanding this limitation.

Fiber coatings are of Hytrel® or similar material. Module must therefore be protected against ultraviolet light exposure.

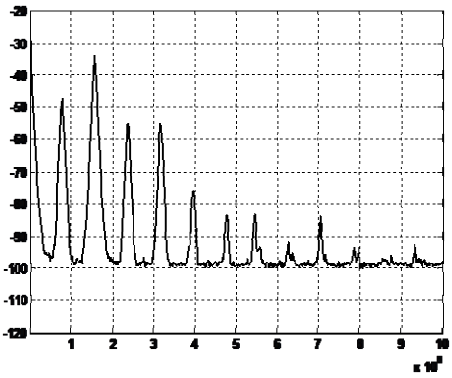
EPS1000 Polarization Scrambler/Transformer

- Ultrafast endless optical polarization scrambling with **40 ns updating intervals**
- Continuous, quasi-steady endless polarization trajectories 0.01 rad/s ... **10000 krad/s** (20000 krad/s with reduced accuracy). **Small steps, e.g., 0.02 rad at 500 krad/s**
- 6 electrooptic quarterwave plates (QWP) and 1 halfwave plate (HWP) with adjustable rotation speeds (QWP: −999999.99 ... +999999.99 rad/s; HWP: −10000.00 ... +10000.00 krad/s)
- Optical frequency can be preset for most accurate waveplate operation, at least from C band to L band (186.2 ... 196.0 THz, 1529 ... 1610 nm). Optional: S band, 1310 nm
- Insertion loss ~1.5 ... 3 dB. Power consumption ~12 W (+5 V power supply 100 ... 240 V included)
- Differential group delay (DGD) sections consisting of polarization-maintaining fibers (PMF) available for highly realistic PMD emulation, using several EPS1000 and DGD sections.
- Available as a desktop unit, module or intellectual property core
- Operation of desktop unit via control buttons or USB (software is included). Several units can be controlled simultaneously by the graphical user interface (see p. 2) or by Matlab™. Speeds of rotating and positions of stopped waveplates and electrode voltages can be set, saved and loaded.
- Serial Peripheral Interface (SPI) for realtime operation; e.g., direct setting of waveplate voltages.
- In synchronous scrambling mode, user-generated tables with sets of waveplate positions can be loaded. Following an external trigger event (3.3 V LVCMOS signal applied at BNC connector, or SPI command) the sets are executed sequentially at specified instants (granularity: 40 ns; minimum delay until next execution instant: 200 ns). Useful for recirculating loop experiments.
- In triggered scrambling mode, the sets are executed cyclically one by one upon external trigger events or USB commands (minimum delay until next execution instant: 200 ns). Application examples: polarization-dependent loss (PDL) and Mueller/Jones matrix measurements.
- **NEW: Optional photodetectors enable accurate PDL and loss measurements**
- EPX1000 = cost-saving desktop unit with combined functionalities of EPS1000 and 40...100 krad/s polarization controller/demultiplexer EPC1000

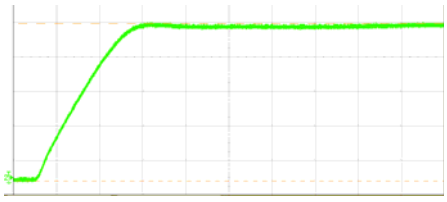


Slow HWP operation — Fast HWP operation

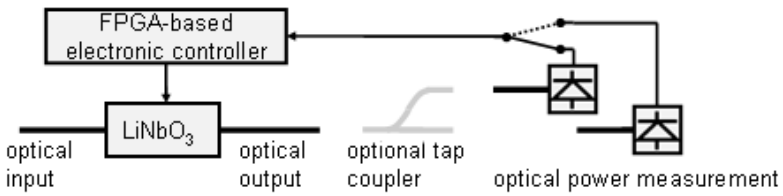
Exemplary output trajectories on Poincaré sphere



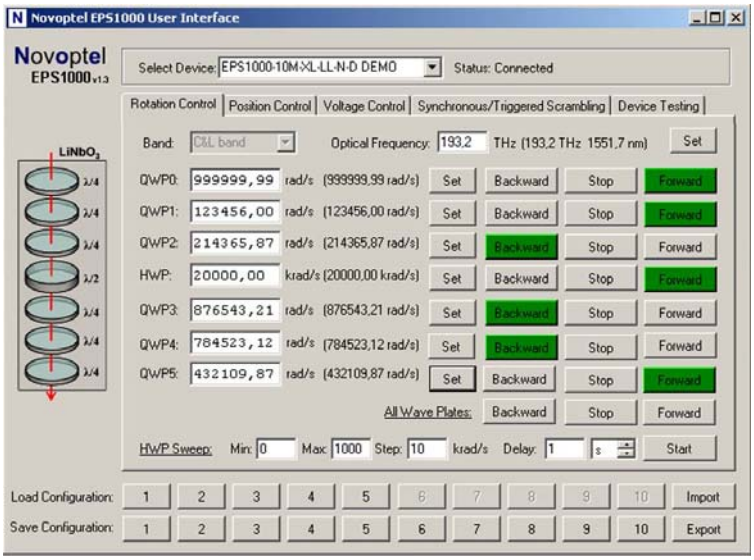
Electrical scrambling spectrum behind polarizer at 10 Mrad/s (horizontal: Hz; vertical: 10 dB/div)

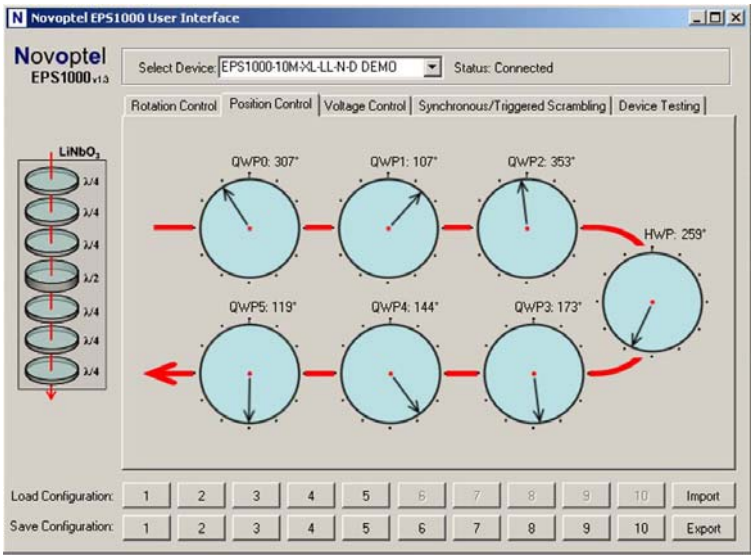


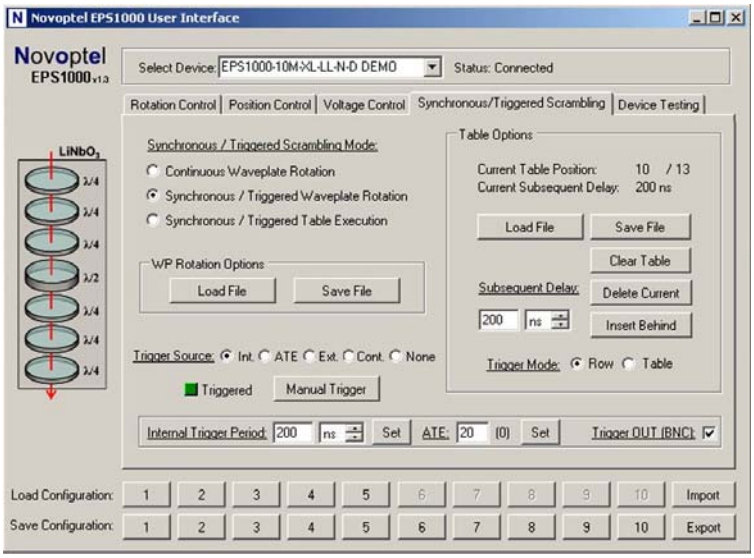
60-V step at HWP settles completely within 50 ns (20 ns/div). Small-signal response is a lot faster.



EPS1000 configuration with optional, electronically switched photodetectors for accurate **PDL and loss measurement**. Optomechanical switch available for device-under-test switching.







Shown are frequently used operation modes of USB-operated graphical user interface.

Other operation modes are:

- Voltage Control: Direct setting of 16 electrode voltages
- Device Testing: Intensity recording for PDL and loss measurement (optional)

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